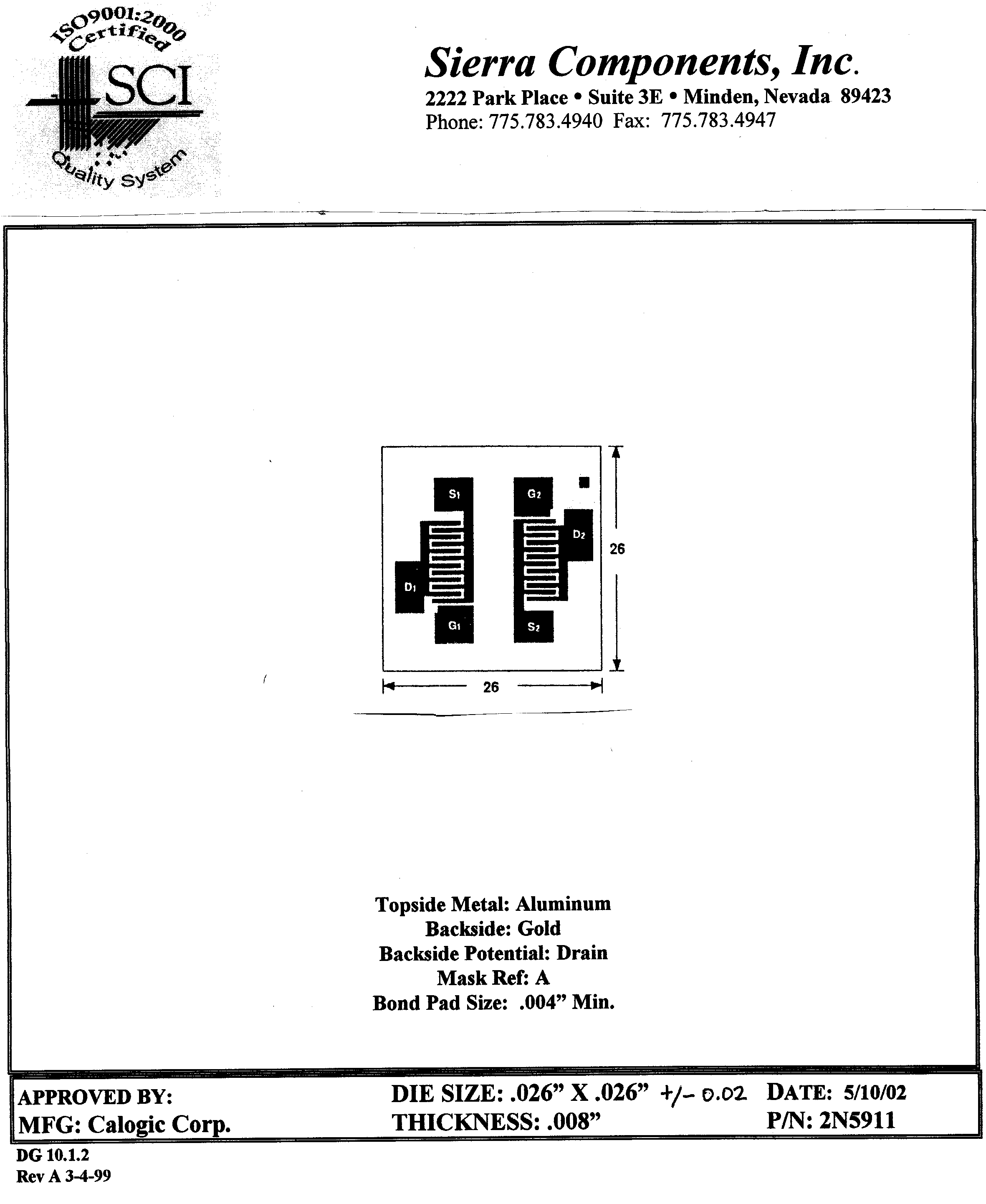
Chip back potential is the level which bulk silicon is maintained by on-chip connection, or it is the level to which the chip back must be connected when specifically stated below. If no potential is given the chip back should be isolated.



**.023”**

**.027”**

**Top Material: Al**

**Backside Material: Au**

**Bond Pad Size: .004” min.**

**Backside Potential: Drain**

**Mask Ref: A**

**APPROVED BY: DK DIE SIZE .023” X .027” DATE: 4/14/16**

**MFG: CALOGIC THICKNESS .008” P/N: 2N5911**

**DG 10.1.2**

#### Rev B, 7/19/02